

DVCon 2010 CALL FOR PAPERS

Conference on Electronic Systems Design and Verification Solutions

February 22-25, 2010

DoubleTree Hotel, San Jose, California, USA

www.dvcon.org



DVCon is the premier conference on the application of languages, tools and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is on the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL SystemC, e, and VERA, as well as general purpose languages such as C and C++. Tools and methodologies include the use of testbench automation, hardware-assisted verification, hardware/software co-verification, assertion-based and formal verification, and transaction-level system design and verification.

Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development, and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using these languages and tools.

TOPIC SUGGESTIONS

We encourage you to contribute your experiences with hardware design and verification languages, advanced tools and methodologies, and to participate in the valuable exchange of ideas.

- Experience using ESL and/or TLM for system-level design and verification
- Experiences deploying a verification methodology library
- Experiences with System-on-Chip design
- Designing and/or verifying complex ASICs and FPGAs
- Using multiple HDLs and/or HVLs in a design cycle
- Techniques for generating constrained-random test, or other automated stimulus generation methods
- Synthesizing transaction-level or abstract designs from high-level languages such as SystemC, System Verilog or C++, to RTL
- Experiences with hardware/software co-design and co-verification
- Experiences with mixed-signal simulation
- Verification techniques that really work (and what did not work)
- Verification process and resource management
- Verification methods that have achieved zero functional bugs in first silicon
- Assertion-based verification
- Coverage-driven verification
- Design and verification IP experiences, good and bad
- Measuring completeness and quality of verification: functional coverage, code coverage or other techniques
- Experience with formal technologies applied to verification, including the application of model checking and simulation together, or the use of dynamic formal verification tools
- Any topic involving the use of an HDL or HVL

CONFERENCE SCHEDULE:

Tuesday, February 23	Wednesday, February 24	Thursday, February 25
• Half-day Tutorials am/pm	• Keynote Address	• Technical sessions
• Exhibition	• Technical sessions	• Panel discussions
	• Panel discussion	
	• Exhibition	

SUBMITTING A PROPOSAL

Paper Proposals: Submit on-line at www.dvcon.org

Panel Proposals: Submit to Stan Krolikoski at stanleyk@cadence.com

Special Session Proposals: Submit to Kathy Emblar at kathy@mpassociates.com

Paper Proposals:

Your proposal should be a short abstract of the paper, one to three paragraphs, 300 to 500 words maximum. The abstract must provide enough detail for the Technical Program Committee (TPC) to evaluate the technical depth and value of your paper. Be creative with your title!

Panel Proposals:

Your proposal should be a short abstract of the panel topic, one to three paragraphs, 300 to 500 words maximum. The proposal should include the proposed panel members. Please provide enough detail for the TPC to evaluate the technical depth and value of your panel.

Special Session Proposals:

Special sessions may consist of embedded tutorials of one to two-hours in length and focused on a specific topic with a list of invited papers/presentations relevant to that topic. Proposals for a special session must contain sufficient information to allow the TPC to assess the quality and interest of the proposal. Special session proposals will be expected to work closely with the TPC to shape and deliver a high-quality session.

AUTHOR'S SCHEDULE:

- **August 10, 2009:** Submission site opens
- **September 14, 2009:** Papers, panels and special sessions due
- **October 5, 2009:** Tutorial proposals due
- **October 28, 2009:** Acceptance notification for all types
- **December 3, 2009:** Complete review draft of papers due
- **January 7, 2010:** Final paper due to proceedings printer

FINAL PUBLICATION REQUIREMENTS

If your proposed paper is accepted, an author kit with details on paper formatting will be sent to you. Final papers should be between four and eight pages, two-column, single-spaced. One author is required to present the paper at the DVCon Conference. A discounted registration fee of \$275 is offered to the presenter of the paper.

SPONSORED BY

The Design and Verification Conference, DVCon, is sponsored by Accellera, www.accellera.org. Accellera is an industry consortium dedicated to the development and standardization of design and verification languages.



For more information concerning the conference, please contact conference management:

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