

DVCon 2010 SPONSORED TUTORIALS

Conference on Electronic Systems Design and Verification Solutions

Tuesday, February 23, 2010

DoubleTree Hotel, San Jose, California, USA

www.dvcon.org



SPONSORED TUTORIAL PROPOSALS:

DVCon is the premier conference on the application of languages, tools and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is on the usage of specialized design and verification languages such as Verilog, SystemVerilog, VHDL, PSL, SystemC, e, and VERA, as well as general purpose languages such as C and C++. Tools and methodologies include the use of testbench automation, hardware-assisted verification, hardware/software co-verification, assertion-based and formal verification, and transaction-level system design and verification.

DVCon is looking for tutorial topics that are current, have a high-level of interest and offer a strong educational content. The DVCon technical program committee will review all tutorials for content prior to publication. **Please include in the proposal the name of the companies that will be sponsoring the tutorial.**

Over 200 qualified engineers attended the sponsored tutorials during DVCon 2009. Tutorial sponsors reached a captive audience during the half-day educational sessions and had the opportunity to follow-up with them during breaks, at the exhibits, and following the event.

DVCon is a highly targeted venue for designers addressing major verification issues. You can position your company at the forefront of these discussions by sponsoring at either the Gold or Silver level. **Email proposals to Stan Krolikoski: stanleyk@cadence.com by October 5, 2009.**

DVCON GOLD TUTORIAL SPONSORSHIP \$17,000

- Distribution of company flyer at sponsored tutorial
- 10 minute commercial presentation during the tutorial
- Company may display sign or hang banner at the tutorial (Banners and signs need to be supplied by the sponsoring company)
- 8x10 booth in the exhibit hall on Tuesday, February 23 - Wednesday, February 24
- Sponsorship of luncheon (based on availability)
- Copy of DVCon 2009 and 2010 attendee list (no email addresses)
- List of registrants that registered for your tutorial (email addresses included)
- Description and logo in Advance and Final Program
- 2 passes to attend the technical program Wednesday, February 24 - Thursday, February 25
- 1 email blast to the DVCon mail list. Company to provide HTML file (Date selection is established by lottery, and is based on availability)

DVCON SILVER TUTORIAL SPONSORSHIP \$10,000

- Distribution of company flyer at sponsored tutorial
- 10 minute commercial presentation during the tutorial
- Company may display sign or hang banner at the tutorial (Banners and signs need to be supplied by the sponsoring company)
- 8x10 booth in the exhibit hall on Tuesday, February 23 - Wednesday, February 24
- Copy of DVCon 2009 and 2010 attendee list (no email addresses)
- List of registrants that registered for your tutorial (email addresses included)
- Description and logo in Advance and Final Program
- 2 session passes to attend the technical program Wednesday, February 24 - Thursday, February 25
- 1 email blast to the DVCon mail list. Company to provide HTML file (Date selection is established by lottery, and is based on availability)

SUGGESTED TOPICS:

- SystemVerilog — Using SV for verification appears to be high interest, but design with SV would also be of interest.
- SystemC (or more generally, C/C++ based) — Design and Verification of systems. Hardware and software or just hardware but at high-levels, etc.
- Assertion-based Verification. (SystemVerilog Assertions, PSL, etc.)
- Coverage-driven Verification.
- Transaction Level Modeling (TLM) and ESL Design including: architectural and algorithmic exploration; interface-based design; using IP-XACT for internal and external IP integration; hardware/software trade-offs and co-verification.
- Principles of modern design verification.
- Moving from proprietary solutions to standards-based solution for design and/or verification. (SystemVerilog, SystemC, PSL all provide the ability for users to move from proprietary methods to standards-based methods.)

TUTORIAL PROPOSAL REQUIREMENTS DEADLINE: OCTOBER 5, 2009

- Expectation of attendee interest to include currency of topic, breadth of appeal and other assessments.
- Educational content and quality of the materials. TPC will have a final review of the presentation materials to ensure that these goals are met.
- Include suggested presenters and biographies.
- Presentation slides need to be supplied in advance of the conference. These will be produced in hard copy format and distributed to all registered tutorial attendees.

TUTORIAL DEADLINES

- October 5, 2009 – Proposals due
- October 28, 2009 – Acceptance/Reject Notification
- January 20, 2010 – Review of presentation slides by the DVCon Tutorial Chair
- February 9, 2010 – Final slides due for printing

SPONSORED BY

The Design and Verification Conference, DVCon, is sponsored by Accellera, www.accellera.org. Accellera is an industry consortium dedicated to the development and standardization of design and verification languages.



For additional information concerning the conference, please contact the conference management:

MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
Telephone: 303-530-4562 Fax: 303-530-4334
Email: kathy@mpassociates.com



CONFERENCE SCHEDULE:

- | Tuesday, February 23 | Wednesday, February 24 | Thursday, February 25 |
|----------------------------|------------------------|-----------------------|
| • Half-day Tutorials am/pm | • Keynote Address | • Technical sessions |
| • Exhibition | • Technical sessions | • Panel discussions |
| | • Panel discussion | |
| | • Exhibition | |

Email proposals to Stan Krolikoski: stanleyk@cadence.com by October 5, 2009.